Amendments to the Drawings:

Replacement Sheets (26 sheets) of drawings containing Figs. 2A, 2B, 2C, 2D, 2E, 3A, 3B, 3C, 4A, 4B, 4C, 4D, 4E, 4F, 4G, 4H, 4I, 4J, 5C, 5D, 5E, 5F, 6, 7A, 7B and 8 are enclosed. These include the drawings as approved by the Examiner in Paragraph 1 on page 2 of the action, and the drawing objections maintained in paragraph 2. The applicants have corrected the reference characters in the description thus avoiding the Examiner's objections.

Attachments: REPLACEMENT SHEETS (26 sheets)

REMARKS/ARGUMENTS

The specification has been amended to correct typographical errors which appeared in the amendment filed January 25, 2005. The specification was further amended on page 45, beginning at line 13 to correct an objection raised by the Examiner in the earlier Office Action of September 8, 2004.

With regard to paragraph 6 (page 3) of the Office Action, a copy of page 27 of the amendment filed January 25, 2005 is attached.

With regard to paragraph 7 (page 3) of the Office Action re "non-responsiveness re: page 48" -- "HDL code 701" has been corrected to read: "HDL code 751".

Claims 83 - 106 are pending in the application.

Claims 1 - 30 have been cancelled, and have been replaced with new claims 83 - 106. Claims 31 - 82 have been cancelled without prejudice.

Claim 1 has been rewritten as new claim 83 and now includes the language: "global scan enable (global_SE) signal and one or more global set/reset enable (global_SR_EN) signals" as set forth in the first two lines of claim 83.

Claims 3 and 19 have been replaced with claim 85 to describe further use of the global enable (global_SE) signal for shift-in and shift-out. This means that there is no additional signal pin requirement using global_SE to enable or disable set/reset testing.

Claim 17 has been rewritten as new claim 96 and now recites: "global scan enable (global_SE) signal and a global set/reset enable (global_SR_EN) signal" as set out in the first two lines of claim 96.

Claim 19 has been replaced with claim 98 which further describes use of the global scan enable (global_SE) signal for shift-in and shift-out. This means that there is no additional signal pin requirement in the global_SE enable or disable set/reset testing.

Reconsideration is respectfully requested of the rejection of claims under 35 U.S.C. §102(b) as being anticipated by Ahanin (US 5,166,604). In the final rejection and the Examiner's response to applicants' argument, the Examiner noted that applicants were arguing features (the (global_SE and global_SR_EN) signals) of the invention which were not recited in the claims. Applicants have now amended the claims to recite these features.

In contrast, Ahanin uses "one" PRESET/CLEAR DISABLE signal to test each asynchronous NPRESET/NCLEAR port (see Fig. 2 in Ahanin). Since a real design can use many PRESET/CLEAR DISABLE signals, Ahanin further disclosed an example test circuit in Fig. 3 to generate these TEST CONTROL SIGNALS. The example test circuit is not perfect because it creates "new" asynchronous set/reset violations (see Q to CLRN in Fig. 3), uses an additional TEST CONTROL pin as the test CLOCK, and introduced a number of non-scan D flip-flops to save the TEST CONTROL SIGNALS. Ahanin does <u>not</u>

point out how to test the newly created set/reset logic (Q to CLRN) and non-scan flip-flops, rendering Fig. 3 not quite practical in real applications.

There is another solution to use a shift register to generate these internal TEST CONTROL SIGNALS, but shifting could potentially destroy the contents of each flip-flop. Ahanin does not teach how to prevent the data from being corrupted due to shifting, though schemes are available using an additional input signal or internal register.

These problems are solved by the present application discovery that using one control signal for testing each asynchronous set/reset port is not good enough; the test circuit hardware is large and the test circuit may not be tested.

In regard to the Examiner's reference to Fig. 2D prior art disclosure in the present application:

This prior art using one global SE to test set/reset is simple because it allows to disable all set-reset during scan shift. The problem is this SE is only one pin, so if there are ripple set/reset circuitries (or loops), a race condition can occur. This will cause significant fault coverage drop and is no longer a practical solution.

Therefore, the present invention uses one global scan enable (global_SE) in addition to using only "one" global set/reset enable (global_SR_EN) signal. See Fig. 3A and Fig. 3B in the present application. See independent claims 83 and 96. The global_SE

signal can globally disable all set/reset ports so that during shifting using the above shift register solution, all flip-flop contents are preserved. Since scan enable is a must for scan-based designs, we need not to use any additional pin for global_SE. In addition, we can shift in all global_SR_EN signals through TDI using the IEEE 1149.1 Boundary-scan Standard when required. Therefore, the present invention virtually does not need any additional input signal pin when each global_SR_EN signal is qualified by the global scan enable (global_SE) signal. And the test circuit hardware is small.

In view of the above, further and favorable reconsideration is respectfully requested.

Respectfully submitted,

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Attachments: RCE
Replacement Sheets of Drawings (26 sheets)
Copy of Page 27 from amendment filed Jan. 25, 2005

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